Advanced Micro Devices

AMD Opteron™ Processor Product Data Sheet

- **Compatible with Existing 32-Bit Code Base**
  - Including support for SSE, SSE2, MMX™, 3DNow!™ technology and legacy x86 instructions
  - Runs existing operating systems and drivers
  - Local APIC on the chip

- **AMD64 Technology**
  - AMD64 technology instruction set extensions
  - 64-bit integer registers, 48-bit virtual addresses, 40-bit physical addresses
  - Eight additional 64-bit integer registers (16 total)
  - Eight additional 128-bit SSE/SSE2/SSE3 registers (16 total)

- **64-Kbyte 2-Way Associative ECC-Protected L1 Data Cache**
  - Two 64-bit operations per cycle, 3-cycle latency

- **64-Kbyte 2-Way Associative Parity-Protected L1 Instruction Cache**
  - With advanced branch prediction

- **1024-Kbyte (1-Mbyte) 16-Way Associative ECC-Protected L2 Cache**
  - Exclusive cache architecture—storage in addition to L1 caches
  - Up to 1 Mbyte per L2 cache

- **Machine Check Architecture**
  - Includes hardware scrubbing of major ECC-protected arrays

- **Power Management**
  - Multiple low-power states
  - System Management Mode (SMM)
  - ACPI compliant, including support for processor performance states

940-Pin Package Specific Features

- **Electrical Interfaces**
  - HyperTransport™ technology: LVDS-Like differential, unidirectional
  - DDR SDRAM: SSTL_2 per JEDEC specification
  - Clock, reset, and test signals also use DDR SDRAM-like electrical specifications

- **Packaging**
  - 940-pin lidded ceramic or organic micro PGA
  - 1.27-mm pin pitch
  - 31 x 31 row pin array
  - 40 mm x 40 mm ceramic or organic substrate
  - Ceramic or organic C4 die attach

- **Integrated Memory Controller**
  - Low-latency, high-bandwidth
  - 144-bit DDR SDRAM at 100, 133, 166, and 200 MHz
  - Supports up to eight registered DIMMs
  - ECC checking with double-bit detect and single-bit correct

- **HyperTransport™ Technology to I/O Devices**
  - Three links, 16-bits in each direction, each supports up to 2000 MT/s or 4.0 GB/s in each direction
  - Each link on uniprocessor (UP) models supports connections to I/O devices.
  - Each link on dual-processor (DP) models supports connections to I/O devices, and any one of the three available links may connect to another DP or MP processor.
  - Each link on multiprocessor (MP) models supports connections to I/O devices or other DP or MP processors.